UNIVERSITY COLLEGE TATI

UNIVERSITY COLLEGE TATI (UC TATI)

FINAL EXAMINATION QUESTION BOOKLET	
COURSE CODE	: BMT 1043
COURSE	: ELECTRONICS
SEMESTER/SESSION	: 1-2024/2025
DURATION	: 3 HOURS

Instructions:

1. This booklet contains 4 questions. Answer **ALL** questions.
2. This Final Exam is an **OPEN BOOK**.
3. All answers should be written in answer booklet.
4. Write legibly and draw sketches wherever required.
5. If in doubt, raise your hands and ask the invigilator.

DO NOT OPEN THIS BOOKLET UNTIL YOU ARE TOLD TO DO SO

THIS BOOKLET CONTAINS 6 PRINTED PAGES INCLUDING COVER PAGE

QUESTION 1

a) A 100 V peak sine wave is applied to the primary winding in Figure 1.

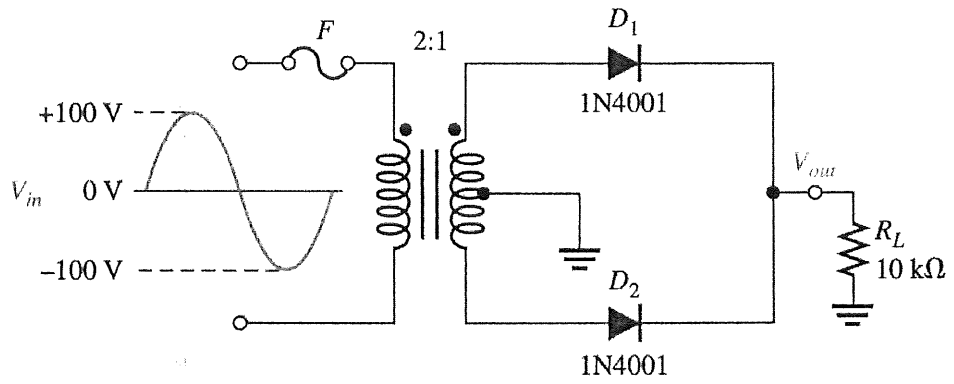

Figure 1

i. Calculate the voltage waveforms across each half of the secondary winding and across R_L. (4 marks)

ii. Draw the voltage waveforms across each half of the secondary winding and across R_L. (3 marks)

b) Refer to diode aplication circuit in Figure 2.

i. Calculate the output voltage, V_{out} across the load resistor, R_L for the complete input cycle. (5 marks)

ii. Draw the output voltage waveform in b(i) (3 marks)

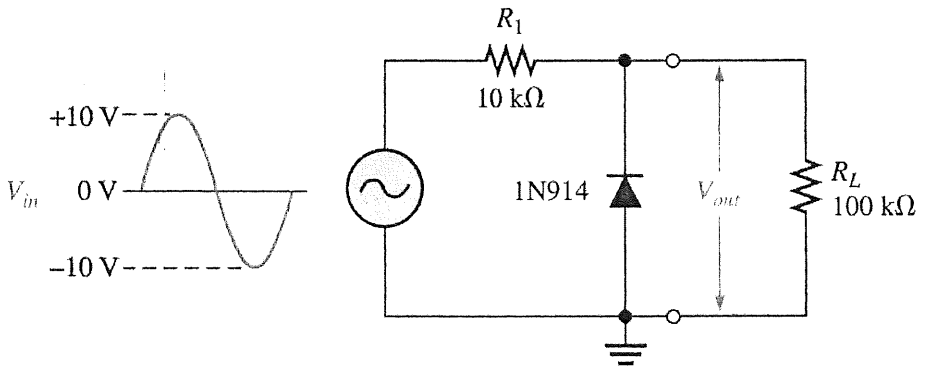

Figure 2

QUESTION 2

a) Given the faulty BJT circuit shown in Figure 3, where the measured collector voltage (V_C) reading with respect to ground is equal to V_{CC} (10V), describe each possible fault for the base voltage and the emitter voltage with respect to ground in Table 1. (10 marks)

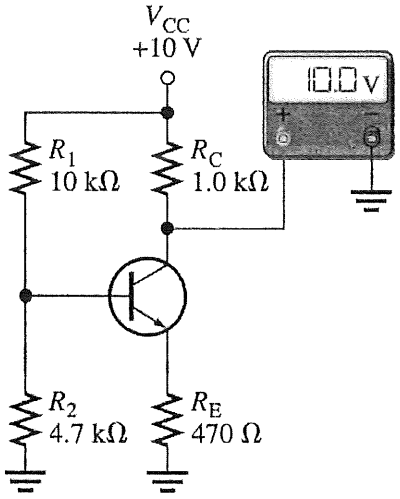

Figure 3

Table 1

Fault	V_c (V)	V_E (V)	V_B (V)
1	10	0	0
2	10	2.50	3.20
3	10	0	3.20
4	10	0	3.20
5	10	0.41	1.11

QUESTION 3

a) Draw the symbol for JFET and MOSFET (2 marks)

b) Draw the biasing circuit for JFET and MOSFET (3 marks)

QUESTION 4

a) For the particular JFET in Figure 4, the parameter values such as g_m, $V_{GS(off)}$, and I_{DSS} are such that a drain current (I_D) of approximately 5 mA is produced.

i. Calculate voltage drain to source, V_{DS} (5 marks)

ii. Calculate voltage gate to source, V_{GS} (2 marks)

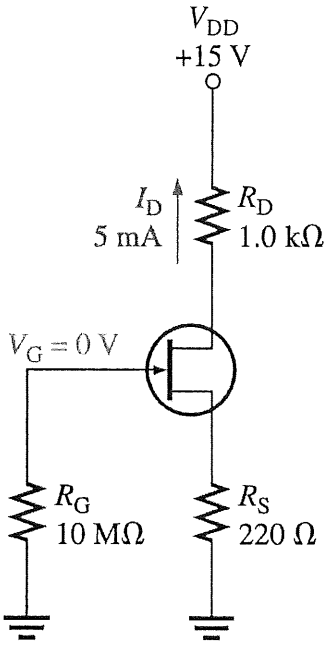

Figure 4

b) Determine the value of RS required to self-bias an n-channel JFET that has the transfer characteristic curve shown in Figure 5 at VGS = -5 V.

(3 marks)

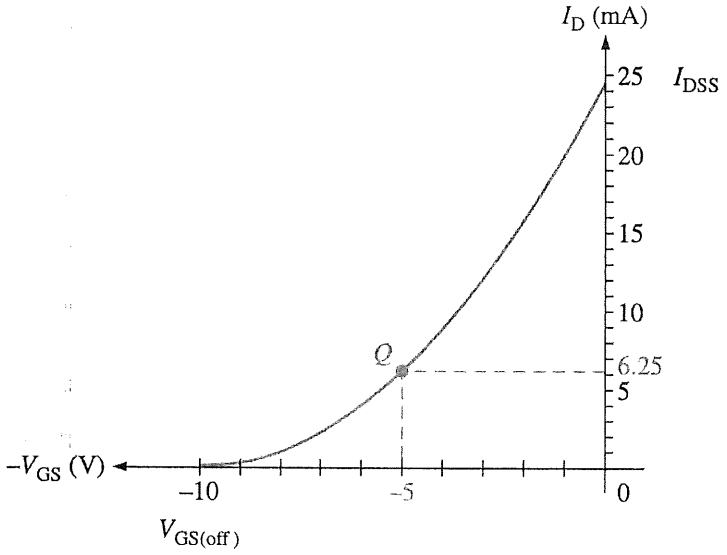

Figure 5

----------End of question----------